In the Claims

Please amend the claims as follows.

1. (Currently Amended) A method, comprising:

executing program instructions from a cache separately in

a normal mode in which only valid instructions having valid results are executed from the cache, and

a run ahead mode in which only future instructions that do not have valid results are speculatively executed from the cache;

determining whether [[a]] the mode is run ahead execution or normal execution; and

upon a cache hit for a first cache line during run ahead execution, setting a protection bit associated with the first cache line.

2. (Original) The method as in claim 1, further comprising:

upon a cache miss for a second cache line during run-ahead execution, evicting an unprotected cache line.

3. (Original) The method as in claim 2, further comprising:

upon a cache miss for the second cache line during run-ahead execution, replacing the evicted cache line with the second cache line and setting a protection bit associated with the second cache line.

4. (Original) The method as in claim 1, further comprising:

upon starting normal execution, clearing all protection bits.

5. (Original) The method as in claim 1, further comprising:

upon starting run-ahead execution, clearing all protection bits.

6. (Previously Presented) A method, comprising:

finding a potential victim in a cache during a run ahead mode separate from a normal execution mode;

determining whether a protection bit is set for the potential victim; and

evicting the potential victim only if the protection bit is clear.

7. (Original) The method as in claim 6, further comprising:

allocating a cache line into the cache to replace the potential victim; and

setting a protection bit associated with the allocated cache line.

8. (Original) The method as in claim 7, further comprising:

switching to normal execution;

referencing the allocated cache line; and

clearing the protection bit associated with the allocated cache line.

9. (Previously Presented) A method, comprising:

determining whether a mode is run-ahead execution or normal execution; and

upon a cache miss during run-ahead execution, replacing a first cache line only if a protection bit associated with the first cache line is clear.

10. (Original) The method as in claim 9, further comprising:

upon a cache hit for a second cache line during run-ahead execution, setting a protection bit associated with the second cache line.

11. (Original) The method as in claim 9, further comprising:

upon a cache hit for a second cache line during normal execution, clearing a protection bit associated with the second cache line.

12. (Currently Amended) A method, comprising:

executing a software prefetching thread concurrently with normal threads in a program on a multithreaded processor, wherein

the normal threads execute only valid instructions that produce valid results, and

the prefetching thread speculatively executes only future instructions that do not produce valid results;

setting protection bits during execution of the software prefetching thread whenever cache lines are allocated and whenever there is a cache hit, the protection bits protecting cache lines from premature eviction; and

clearing protection bits during execution of the normal threads as cache lines allocated for the software prefetching thread are referenced by the normal threads.

13. (Original) The method as in claim 12, further comprising:

clearing all protection bits when the software prefetching thread finishes executing.

14. (Original) The method as in claim 12, further comprising:

spawning the software prefetching thread for a predetermined section of code in the program.

15. (Original) The method as in claim 14, further comprising:

providing code for a software prefetching thread from an optimizing compiler.

16. (Currently Amended) A processor, comprising:

a cache having a plurality of cache lines;

a plurality of registers to store data for instructions to be executed by the processor;

execution logic to execute program instructions separately in a normal mode in which only valid instructions having valid results are executed from the cache, and speculatively in a run ahead mode in which only future instructions that do not have valid results are executed from the cache;

~~circuitry to load data from the cache to the plurality of registers;~~

circuitry to prefetch data during [[a]] the run ahead mode ~~separate from a normal processing mode~~, and to allocate cache lines to store the data; and

a plurality of identifiers associated with each cache line, each identifier to indicate whether to protect an associated cache line from premature eviction during the run ahead mode.

17. (Previously Presented) The processor as in claim 16, wherein
at least one of the plurality of identifiers is adapted to indicate whether the associated cache line is still in use.

18. (Previously Presented) The processor as in claim 16, wherein
at least one of the plurality of identifiers is adapted to indicate whether the associated cache line was allocated during the separate run ahead mode and has yet to be touched during the normal execution mode.

19. (Original) The processor as in claim 15, the cache further comprising:
a cache data memory; and
a cache directory to determine hits or misses and to store address tags of corresponding cache lines currently held in the cache data memory, the cache directory to store the identifiers.

20. (Original) The processor as in claim 15, the cache further comprising:
a cache controller to implement a cache strategy for moving data into and out of the cache data memory and the cache directory, the cache controller to store the identifiers.

21. (Currently Amended) A multiprocessor computer system, comprising:
a plurality of processors, each one of the processors having prefetcher logic and being capable of speculative execution during a run ahead mode which executes only invalid instructions and produces invalid results;
at least one main memory;

at least one communication device coupling the plurality of processors to the at least one main memory;

a plurality of caches having a plurality of cache lines, each one of the plurality of caches associated with one of the plurality of processors; and

a protection bit associated with each of the cache lines in each of the plurality of caches, each protection bit to protect a cache line from premature eviction during speculative execution.

22. (Original) The multiprocessor computer system as in claim 21, further comprising:
control logic associated with the plurality of caches to manage the protection bits.

23. (Original) The multiprocessor computer system as in claim 22, further comprising:
at least one cache controller associated with the plurality of caches;
wherein the control logic resides in the at least one cache controller.

24. (Original) The multiprocessor computer system as in claim 21, further comprising:
a plurality of tag arrays associated with each cache;
wherein the protection bits reside in each tag array associated with each cache.

25. (Currently Amended) A computer system, comprising:
a main memory;
a processor having
a run ahead mode in which it speculatively executes only future instructions that do not produce valid results, and
~~separated in time from~~ a separate normal execution mode in which it executes only valid instructions that produce valid results;
a bus to connect the main memory and the processor;
a cache associated with the processor, the cache having a plurality of cache lines; and
a protection bit associated with each of the cache lines in each of the plurality of caches, each protection bit to protect a cache line from premature eviction during processor operation in the run ahead mode.

26. (Original) The computer system as in claim 25, wherein the cache is a level one (L1) cache.

27. (Original) The computer system as in claim 26, wherein the level one (L1) cache is on the same chip die as the processor.

28. (Original) The computer system as in claim 25, wherein the cache is a level two (L2) cache.

29. (Currently Amended) A computer readable storage medium bearing instructions for carrying out a method comprising:

executing program instructions from a cache separately in

a normal mode in which only valid instructions having valid results are executed from the cache, and

a run ahead mode in which only future instructions that do not have valid results are executed from the cache;

determining whether [[a]] the mode is run ahead execution or normal execution; and

upon a cache hit for a first cache line only during run ahead execution, setting a protection bit associated with the first cache line.

30. (Previously Presented) The medium as in claim 29, the method further comprising:

upon a cache miss for a second cache line during run-ahead execution, evicting an unprotected cache line.

31. (Previously Presented) The medium as in claim 30, the method further comprising:

upon a cache miss for the second cache line during run-ahead execution, replacing the evicted cache line with the second cache line and setting a protection bit associated with the second cache line.